REMARKS

Claims 1-17 are pending in this application.

Claims 1-17 are rejected.

The office action dated June 29, 2006 indicates that base claim 1 is rejected under 35 USC §112, second paragraph, because the phrase ", the read circuit including a digital counter having an output that indicates a single bit" is unclear. This rejection is respectfully traversed. When claim 1 is read in view of the specification, there is no confusion as to the meaning of the phrase. See, for example, paragraph 3 (the single bit is the MSB) and paragraph 24 (the single bit is the sign-bit of digital counter 120). Nevertheless, claim 1 has been amended for clarity.

The office action also indicates that claims 2 and 5 are rejected under 35 USC §112, second paragraph, because claim 2 appears to be missing a verb, and claim 5 recites "store" instead of "stored." These rejections are respectfully traversed because claim 2 is not missing a verb, and it is quite clear to the examiner that the applicants meant "stored" instead of "store" in claim 5. The examiner is thanked for identifying the typo in claim 5, which has been corrected by the amendment above.

The office action indicates that base claim 1 is rejected under 35 U.S.C. §103 as being unpatentable over Baker U.S. Patent No. 7,009,901. The office action contends that the read circuit of claim 1 is obvious in view of the read circuit 200 in Baker's Figure 2. This rejection is respectfully traversed.

Amended claim 1 recites a data storage device comprising non-volatile memory, and a read circuit including a digital counter for storing an n-bit count, where n>1. The digital counter has an output that indicates a single bit of the

count (e.g., the sign bit). During a read operation, the read circuit performs multi-sample read operations on the memory.

Paragraph 4 of the specification identifies a shortcoming with this type of counter: the full contents of the counter are not made available, since the output only indicates a single bit of the count. Paragraph 5 of the specification explains why it is sometimes desirable to know the contents of the counter.

This shortcoming is addressed by claim 1. Claim 1 further recites that the read circuit has a test mode of operation. During the test mode, the read circuit allows test clock pulses to be applied to the digital counter. The test clock pulses can be counted to determine a state of the digital counter.

Baker does not recognize this shortcoming, nor does Baker offer a solution that addresses this shortcoming. The reason is clear: Baker does not disclose the type of read circuit recited in claim 1.

During a read operation with Bakers read circuit 200, a sense amplifier 202 senses the logic state of a selected memory cell, and generates a pulse train (col. 3, lines 32-34). Frequency of the pulse train is determined by the logic state (col. 2, lines 34-36). A counter 204 counts the pulses (col. 3, lines 36-38). The stored count (SCNT) in the counter 204 represents the logic state of the selected memory cell.

During the read operation, a signal LC is asserted every T seconds (col. 3, lines 40-47). When the signal LC is asserted, the full count SCNT (all bits) in the counter 204 is latched and compared to a reference count RCNT (col. 3, lines 47-51). The comparison indicates whether a logic ‘1’ or a logic ‘0’ is stored in the selected memory cell (col. 3, lines 51-56).

All of these steps are performed during a single mode of operation. Baker does not teach or suggest two separate modes of operation.

During Baker's single mode of operation, only a single sample is taken. [1] In contrast, the read circuit of claim 1 takes multiple samples.

During Baker's read operation, the full contents of the counter 204 are latched and compared. In contrast, only a single bit is provided by the counter of claim 1. Thus, Baker's counter does not have the shortcoming described above.

Baker doesn't teach, hint or remotely suggest the need to determine the state of his counter 204. Baker offers no reason, incentive or motivation for supplying test pulses to the counter.

Moreover, pages 4-5 of the office action acknowledge that Baker doesn't disclose a test mode. However, the examiner does not cite a description of a test mode in the prior art, nor does the examiner cite reason, incentive or motivation in the prior art for adding a test mode to Baker's device. All the examiner offers is an unsubstantiated allegation of obviousness. Presumably, the allegation is based on the personal knowledge of the examiner.

The unsubstantiated allegation is hereby challenged. The examiner is respectfully requested, pursuant to MPEP §707 and 37 CFR §1.104(d)(2), to cite a document or affidavit supporting her personal knowledge.

Baker alone does not provide evidence of prima facie obviousness of claim 1. Therefore, claim 1 and its dependent claims 2-9 should be allowed over Baker.

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[1] In the rejection of claim 3, the examiner alleges that a multi-sample operation is disclosed at col. 3, lines 30-40 because the sense amplifier is used to determine SCNT and RCNT. However, lines 30-40 say no such thing. Lines 30-40 describe the generation of a single sample

The office action indicates that bases claims 9, 10, 15 and 16 are rejected under 35 U.S.C. §103 as being unpatentable over Baker. These rejections are respectfully traversed.

Claim 9 recites a read circuit for a memory device. The circuit comprises first means for performing a multi-sample read operation on the memory device, the first means including a digital counter, an output of the digital counter indicating a sign-bit; and second means for allowing contents of the digital counter to be determined by an external device at least one of during and after the multi-sample read operation.

As discussed above, Baker's read circuit does not perform a multi-sample operation, it performs a single sample operation. Moreover, Baker doesn't teach or suggest a need to determine the state of his counter 204 , let alone a means for doing so. Baker is only concerned about whether the count SCNT is higher or lower than threshold RCNT. For these reasons, claim 9 should be allowed over Baker.

Claim 10 recites a method of using a memory device. The method comprises performing a multi-sample read operation on the memory device. The multi-sample read operation includes a plurality of sense operations on the memory device. A digital counter is used during the multi-sample read operation to generate a running sum of values. Each value represents a resistance that was sensed during one of the sense operations.

The method further comprises determining the state of the digital counter during or after the multi-sample read operation, wherein determining the state includes sending clock pulses to an input of the digital counter until a change in a

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(represented by SCNT). Moreover, lines 30-40 are silent about using a sense amplifier to determine RCNT. According to col. 3, lines 51-53, RCNT is simply a threshold.

sign-bit of the digital counter, and counting the clock pulses that were sent to the digital counter.

As discussed above, Baker does not teach a multi-sample operation, it describes a single sample operation. Further, Baker does not teach or suggest keeping a running sum of values, where each value represents a resistance that was sensed during a read operation. That is, Baker does not teach or suggest a running sum of sampled values. Baker's SCNT represents the resistance that was sensed during a single sense operation, since SCNT is reset after each read operation by asserting signal LC (col. 3, lines 47-48). Still further, Baker doesn't teach or suggest a need to determine the state of his counter 204, let alone an approach for doing so. Baker is only concerned about whether the count SCNT is higher or lower than threshold RCNT. For these reasons, claim 10 should be allowed over Baker.

Claim 15 recites a memory tester including a source for generating test clock pulses, a circuit for determining when a sign-bit changes, and a counter for counting the test clock pulses until the sign-bit changes. The examiner does not find evidence of a memory tester in the prior art, let alone the memory tester of claim 15. On pages 3-4 of the office action, the examiner describes how Baker's circuit 200 performs a single sample read operation. However, pages 3-4 do not describe a memory tester, nor do these pages offer a reason, incentive or motivation for testing a counter in a read circuit of a memory device.

Baker doesn't teach or suggest a need to determine the state of his counter 204, let alone a memory tester for determining it. Baker is only concerned about whether the count SCNT is higher or lower than threshold RCNT. Because prima facie obviousness of claim 15 has not been established, the '103 rejections of claim 15 should be withdrawn.

Claim 16 recites an apparatus for externally testing a non-volatile memory device including a digital counter. Baker doesn't teach or suggest such an apparatus. Baker does not teach or suggest means for examining the output of a digital counter to determine when the sign-bit changes. Baker is only concerned with a comparison of SCNT to RCNT.

Baker does not teach or suggest means for counting a number of test clock pulses supplied to the counter input, the count being stopped when the sign-bit changes. Baker's counter stops counting every T seconds, when signal LC is asserted.

Baker does not teach or suggest means for using the count of test clock pulses to determine a performance parameter of the non-volatile memory.

Pages 3-4 of the office action only describes a single sample read operation. It does not discuss these means in particular, or a memory tester in general. Because prima facie obviousness of claim 16 has not been established, the '103 rejections of claim 16 should be withdrawn.

Claims 5-6, 11-14 and 17 are also rejected under 35 U.S.C. §103 as being unpatentable over Baker. The rejections of claims 5-6 are unclear. The examiner copies these claims into the office action, but does not explain why they are rejected. If these rejections are maintained, reasons for the rejections are respectfully requested.

The rejections of claims 11-14 are also unclear. The examiner copies a passage out of Baker that describes a single sample read operation. However, the examiner does not explain why claims 11-14 read on this passage. The examiner does not explain how the passage relates to access time (claim 11), margin (claim 12), using the memory device to establish a reference count (claim

13), or integration time (claim 14). If these rejections are maintained, explanations are respectfully requested.

The rejection of claim 17 is no more than a bald conclusion of obviousness. No prior art is cited. Presumably, the allegation is based on the personal knowledge of the examiner. The unsubstantiated allegation is hereby challenged. The examiner is respectfully requested, pursuant to MPEP §707 and 37 CFR §1.104(d)(2), to cite a document or affidavit supporting her personal knowledge. Baker alone does not provide evidence of prima facie obviousness.

Claim 18 has been added. Claim 18 depends from claim 1. Claim 6 has been amended to depend properly from amended claim 1. Claim 16 has been amended to correct a minor omission.

The examiner is respectfully requested to withdraw the claim rejections. The examiner is encouraged to contact applicant's attorney Hugh Gortler to discuss any issues that might remain.

Respectfully submitted,

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Date: October 20, 2006